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Improving the reliability of silicon diodes via manufacturing process modification strategies

S. Román-Sánchez [a,*], M. París Ogáyar [a,b,c], I. Lorite [d], J.F. Fernández [a], A. Serrano [a], A. Moure [a]

[a] Instituto de Cerámica y Vidrio, CSIC, Kelsen, 5, 28049, Madrid, Spain
[b] Fluorescence Imaging Group, Departamento de Física de Materiales, Facultad de Ciencias, Universidad Autónoma de Madrid, 28049, Spain
[c] IMDEA Nanociencia, C/Faraday, 9, 28049, Madrid, Spain
[d] SEG Automotive Germany GmbH, Lotterbergstraße 30, 70499, Stuttgart, Germany

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ABSTRACT

The multicomponent nature of power electronic devices can be an issue for their reliability due to the high currents and temperatures reached during operation. Proper design of each component and the system as a whole is mandatory to ensure a long lifetime and small failure rates. In this work, we systematically investigate the influence of manufacturing on the behavior of press-fit rectifier Si diodes by introducing changes in the manufacturing process. Concretely, we focused on the solder geometry and the epoxy component. Thermography measurements and computational modeling show that optimization of the solder thickness and its uniformity allows the diode to bear higher currents and temperatures close to 250 °C in the hottest parts of the device (located in the epoxy zones) without failure. In addition, choosing an adequate epoxy with a limited expansion rate over a wide temperature range helps to reduce stress and strain effects, preventing the breakdown of the diodes even at continuous currents up to 40 A.

1. Introduction

Press-fit rectifier diodes [1] are key devices in the alternator of vehicle engines. They are placed in the rectifier bridge in such a way that allow the transformation of the AC signal into a DC one, which is essential for the adequate power supply of the vehicle. During operation, they work in forward bias in each semi-cycle and reverse condition in the other one. In the former working mode, high currents in the order of tens of amperes flow through the diodes with no noticeable increase in voltage, while in the latter situation, they must be capable of working at tens of volts before the current runaway (and, consequently, the reverse breakdown) occurs, leading to the device failure. In both cases, the diode endures a high-temperature increase [2,3] that, if not minimized, results in its lifetime reduction and eventually its final failure.

It is known that semiconductors are a highly vulnerable part of a power electronic system [4]. The mechanisms favoring their failure can be related to the package (understood as all the components of the device that surround or contain the semiconductor) or to the semiconductor chip itself [5] due to effects such as primary or secondary reverse breakdown processes, overstresses caused by overcurrent or overvoltage, or localized charge effects. Proper design device can minimize both types of failures (chip and package). Specifically, in the case of press-fit diodes, three main components besides the silicon wafer can be optimized in order to improve the device performance: metallic heat sink, solder, and epoxy [3].

Regarding the heat sink, it is built with copper-based pieces with sizes limited only by the space availability in the specific application, as can be the size of the alternator. Its shape and volume, among other factors, may determine the ease with which this material releases heat. In the case of the solder (composed of Pb and Sn), several mechanisms lead to its degradation or final failure. Phenomena such as electromigration resulting from high-density currents [6,7] cause the solder-semiconductor matter diffusion, yielding failures. In addition, one of the major causes of solder degradation takes place during the thermal cycling that the device endures during working conditions. Solders provide electrical connections among different parts of the devices and bond different components that, in general, have dissimilar coefficients of thermal expansion (CTE). Differences between the CTE of components cause the appearance of stresses and, consequently, strain in the structure of the material [8], which may result in the formation of cracks that diminish the electrical and thermal conductivity, thereby reducing the lifetime of the device. Such mechanical fatigue issues are

* Corresponding author.
E-mail address: sara.roman@icv.csic.es (S. Román-Sánchez).

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favored by the temperature increase that typically occurs in this type of device during operation at high currents [9,10]. In this sense, the thermal resistance should be minimized or, at least, controlled by the adequate choice of solder dimensions (area and thickness) [11] during manufacturing. This selection allows us to obtain thermal, electrical, mechanical, and economic properties that maximize the functionality and lifetime of the diode. Concerning the epoxy, its low thermal conductivity hinders the heat flow from the semiconductor to the heat sink, which is critical for diode overheating. The epoxy also plays a fundamental role in the heat release from the semiconductor, as we have probed in previous works [3]. In particular, two physical properties of the epoxies in the press-fit diodes are of major importance to avoid the failure of the device [12,13]. The first one is the thermal conductivity, which is intrinsically low for most epoxies and could be improved by the use of different fillers [14–16]. A high thermal conductivity provides a higher heat release from the semiconductor. The second property to be emphasized is the CTE, for which low values are desired in order to guarantee good bonds with the rest of the components in heating-cooling cycles, avoiding detachment. Nowadays, the application and research on the effect of epoxies on the performance of electronic devices is quite wide [17–19].

In this work, the improvements achieved in press-fit silicon diodes by changes in the manufacturing and design of two fundamental components, i.e., the solder and the epoxy, have been monitored to prove a better performance in terms of thermal behavior. For that, three commercial diodes with variations in selected components during the fabrication process have been compared. Important enhancements in their thermal response and reliability are verified by carrying out infrared thermographic experiments and simulations using COMSOL Multiphysics® software. The findings reveal that improving the design by selecting appropriate solder dimensions and replacing diode components, such as epoxy, leads to enhanced thermal and electrical properties. This optimization not only maximizes the functionality and lifetime of the devices but also contributes to economize the product.

2. Experimental procedure

2.1. Experimental characterization

Three commercial diodes with differences in the manufacturing process have been investigated. In all cases, the forward voltage rating is 0.7 V and the maximum forward intensity is 50 A. A general optical view indicating the location of the different components of the diode (Cu-sink, Si wafer, solder, and epoxy) is shown in Fig. S1 of the supporting information. Based on the design of a commercial diode, denoted as Process A, changes in its fabrication have been carried out. The first one is focused on optimizing the manufacturing process itself to achieve an increase in the thickness and uniformity of the solder that joins the silicon chip and the heat sinks. This process has been named as Process B. The second modification, defined as Process C, is performed by replacing the epoxy used in Processes A and B with another epoxy with a lower CTE and improved composition.

Regarding the characterization techniques employed, optical microscopy was used to evaluate the solder thickness and homogeneity of diodes obtained by Processes A and B, using a Zeta-20 Optical Profilometer microscope from Zeta Instruments. Measurements were carried out on the cross-sections of diodes previously cut in half, after a multi-step metallographic polishing process that finishes with 1 μm diamond paste in a Buehler Vibrometer 2 polisher.

Dilatometry and thermogravimetry analysis (TGA) were performed for the epoxies of the diodes obtained by Process A and C, from room temperature (RT) to 400 °C. For dilatometry, the heating microscopy model HR18 from Axel Hesse Instruments was employed while thermogravimetric measurements were carried out with a Netzsch STA 409/C device.

Thermography experiments were carried out in entire diodes using an infrared thermal camera (model FLIR T440, with a focal plane array detector of sensor size 320 × 240, spectral range from 7.5 to 13 μm, and NETD <0.045 °C at 30 °C). Each pixel of the image corresponds to a temperature measured from the infrared signal. A continuous movie was recorded at 30 frames per second, giving a temporal resolution of approximately 0.3 s. The electrical signal was supplied by a TTi QPX1200L power supply for two types of experiments. For the first experiment, a continuous current of 40 A in direct polarization was abruptly applied to the diodes for 15 min or up to the failure of the devices, if this event occurred first. That is, the intensity is not applied gradually, but by direct application of the corresponding voltage to reach such intensity, which occurs in times of approximately 1 s. For the second experiment, thermal cycles were carried out, reaching maximum temperatures of about 250 °C by applying the corresponding current for 2 min. Then, diodes were freely cooled in an air atmosphere for 2,5 min. The temperature was monitored at the external epoxy component close to the socket and the wire. In all cases, diodes were characterized at forward conditions and were denoted as positive or negative depending on whether the current was injected through the head or the wire, respectively, which depends on the semiconductor specifications.

2.2. Modeling and simulation

The simulation of heat distribution across the press-fit diodes varying the process was performed using COMSOL Multiphysics ® Software v. 5.4 (www.comsol.com, Stockholm, Sweden, 2018) in a 3D scheme under specific conditions detailed in the following.

2.2.1. Geometry, materials and meshing

The diode geometry was modeled in a 3D mesh made of an outer sink head copper layer contacting mineral-filled epoxy material, simulating the design and composition of the experimental commercial devices. The epoxy encapsulates the silicon chip, which has PbSn4 solder on top and bottom joined to a copper region with a cylinder wire passing through the epoxy. Dimensions and draws are shown in Fig. 1a.

The material properties for both electric current and heat transfer in the solids module of COMSOL Multiphysics® software were either extracted from the software's own library or added manually. Commercial values were used for solder parameters [20]. A doped silicon chip with a resistivity value of $9.5 \cdot 10^3$ S/m was used for the modeling. This resistivity value was adjusted to reach approximately 250 °C by Joule effect heating at the center of the silicon chip, after a current injection of 40 A for 50 s following the experimental measurements carried out in this work. Finally, epoxy parameters were taken from the literature [21–25]. For simplicity, all parameters used for the modeling were considered as not temperature-dependent.

The mesh applied to the system was physically controlled with a predefined finer size. Fig. 1b shows the mesh of the structure.

2.2.2. Physics

Electric current interface was used to compute currents in conductive media solving a current conservation equation based on Ohm's law, using an electric potential as the dependent variable (V). The static form of the equation of continuity is [26]:

$$\nabla \cdot \boldsymbol{J} = -\nabla \cdot (\sigma \nabla V - \boldsymbol{J}_e) = 0 \qquad (1)$$

where J is the current density [A/m^2], σ is the electrical conductivity [S/m] and J_e is the electric current density due to external sources [A/m^2].

Initial values of V = 0 V were set. A current injection through the outer sink head copper was fixed at 40 A. Finally, the ground was set at the bottom of the copper wire. Thus, the diode notation is positive.

Heat transfer in solids interface in time-dependent mode was added to evaluate heat distribution and temperature profile across the diode as a function of time. The differential equation of conduction is given by:

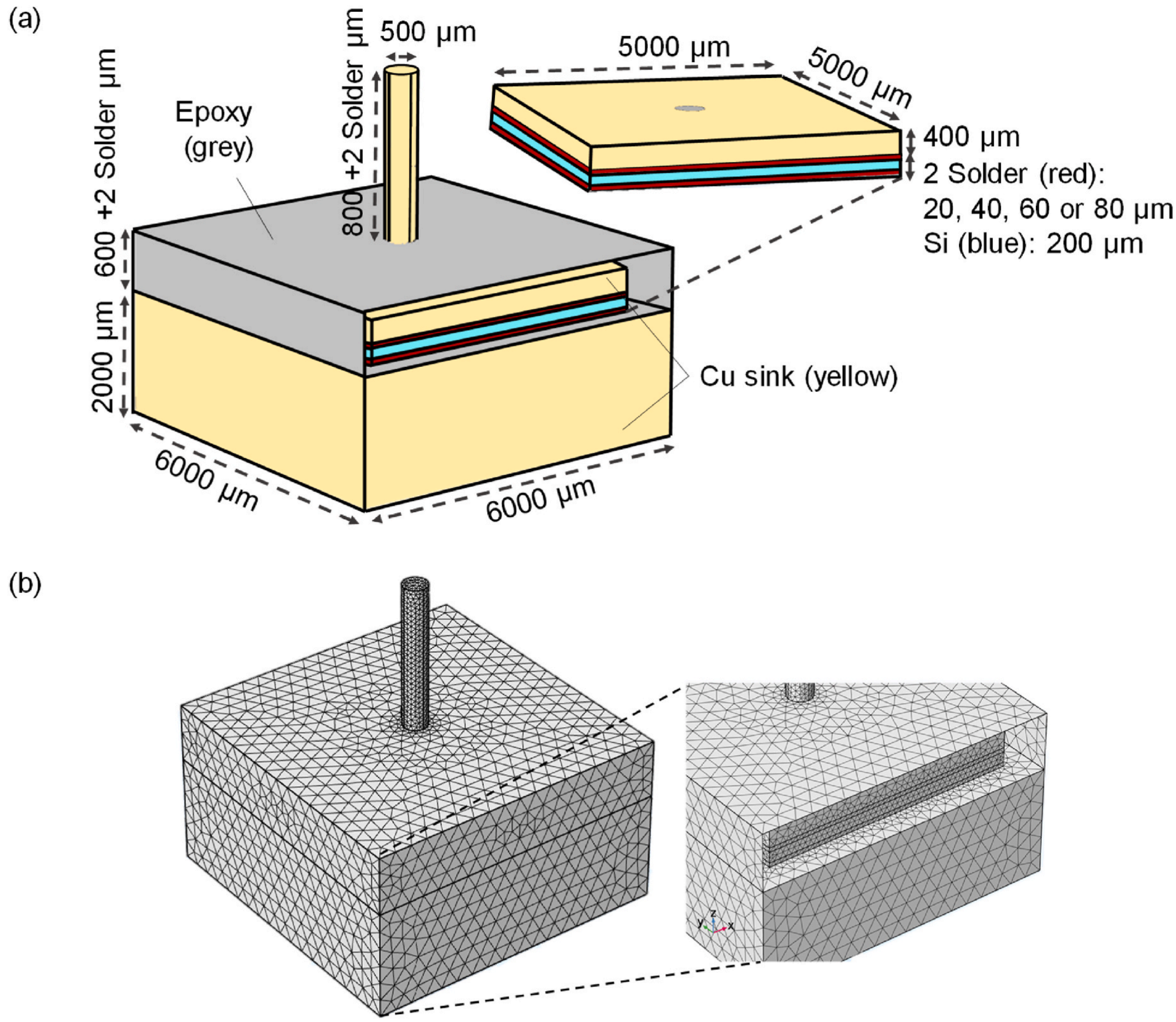

Fig. 1. **(a)** Schematic of the geometry for the considered press-fit diode in 3D, indicating the different components, and **(b)** meshed structure.

$$-k\nabla^2 T + Q = \rho C_p \frac{\partial T}{\partial t} + \rho C_p \nabla T \qquad (2)$$

where k, ρ, C_p, and Q are the thermal conductivity [W/(m·K)], density [kg/m^3], specific heat at constant stress [J/(kg·K)], and the local heat generation rate or source term [W/m^3], respectively. For the simulation, we assume that the entire geometry of the diode is initially at RT.

To consider heat dissipation, a heat flux node across the outer boundaries (copper and epoxy boundaries) of the device was implemented. A heat transfer coefficient was considered with standard ambient flow conditions with a value of h = 5 W/(m^2·K). For the final Joule heating effect, the two physics interfaces (electric currents and heat transfer in solids) were coupled in the Multiphysics branch of the COMSOL platform through electromagnetic heat sources and temperature coupling. A time-dependent study was evaluated from t = 0 s to t = 50 s with a time step of 1 s.

3. Results and discussion

3.1. Influence of solder and epoxy characteristics

The solder thickness of cross-sectioned diodes has been measured in three regions, indicated in Fig. 2) in order to evaluate their uniformity. A more detailed image of a cross-sectioned press-fit diode is shown in Fig. S1 of the supporting information. Concretely, four diodes manufactured by Process A and four diodes manufactured by Process B were

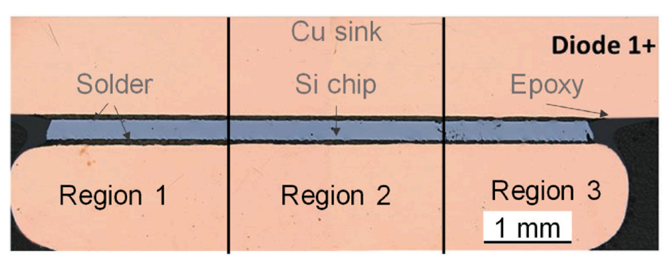

Fig. 2. Cross-sectional optical image of a positive diode manufactured by Process A (as representative), indicating the three regions where the solder thickness was measured and the different constituents of the device.

studied. In both cases, two diodes of each have a positive configuration (denoted with a positive sign, i.e., 1+, 2+) and the other two have a negative configuration (denoted with a negative sign, i.e., 1-, 2-). As explained in the experimental section, positive or negative configuration depends on the orientation of the Si chip. When it is positive, the current flows from the head to the wire, meaning the positive reagion is near the head socket. Contrary, when the diode is negative, the current flows from the wire to the head, meaning the positive region is near the wire. IAiming to achieve more accurate values, five measurements were carried out in each region and averaged. Results are presented in Table 1.

Measured **s**older thickness values have significant differences depending on the processing type. For Process A, the global averages of

Table 1
Averaged solder thickness values measured on diodes manufactured by Process A and B in the three different regions for the upper and bottom solder.

		Process A			
		Region 1 [μm]	Region 2 [μm]	Region 3 [μm]	Average [μm]
Diode 1+	Upper solder	42(2)	28(2)	37(3)	*39(3)*
	Bottom solder	47(1)	40(6)	28(6)	*38(10)*
Diode 1-	Upper solder	37(4)	34(2)	37(2)	*35(2)*
	Bottom solder	32(1)	30(1)	35(2)	*32(3)*
Diode 2+	Upper solder	31(3)	42(5)	59(6)	*44(14)*
	Bottom solder	45(2)	45(1)	49(4)	*46(2)*
Diode 2-	Upper solder	25(2)	20(3)	18(2)	*21(4)*
	Bottom solder	10(2)	14(2)	18(3)	*14(4)*
		Process B			
Diode 1+	Upper solder	27(3)	28(2)	30(2)	*28(2)*
	Bottom solder	23(1)	20(5)	25(3)	*23(3)*
Diode 1-	Upper solder	34(1)	36(3)	37(2)	*36(2)*
	Bottom solder	35(2)	37(3)	43(2)	*38(4)*
Diode 2+	Upper solder	39(2)	41(2)	35(3)	*38(3)*
	Bottom solder	32(5)	37(2)	35(1)	*35(1)*
Diode 2-	Upper solder	31(4)	29(6)	24(2)	*28(4)*
	Bottom solder	33(4)	23(3)	28(4)	*28(5)*

the solder thickness reveal a high dispersion level between diodes, with values from 14 μm to 46 μm and a difference of more than 30 μm. In addition, in some cases, the solder shows thickness gradients within the diode itself and even within the same region (see dispersion between brackets). Contrary, the solder thickness distribution is much more homogenous for Process B, as the values are quite similar regardless of the diode and measurement region. In addition, the dispersion values are much lower. These findings confirm that Process B yields solder joints with a more uniform thickness over their entire length compared to Process A.

The second major change among processes shown in this study is the use of a different epoxy in Process C, which presents the same solder as the one used in Process B. The epoxy should be designed to bear thermal cycling at working conditions during turn on/off of the device where it will expand and shrink. Fig. 3 shows the thermogravimetric measurements of the epoxies for both processes (Process A and C). The onset for weight loss (1 % wt loss) is observed at lower temperatures for the epoxy of Process A (313 °C) than for Process C (326 °C) in Fig. 3a. This weight loss is related to irreversible epoxy degradation by melting. Fig. 3b and c show the dimensional change behavior of the epoxies measured by heating microscopy. In both cases, a first thermal expansion occurs up to a certain temperature, after which the material shrinks. Contraction takes place up to temperatures where faster expansion associated with the thermal degradation of the epoxy occurs. A remarkable difference is observed between both epoxies. The expansion before irreversible degradation is only 0.01 % for the epoxy from Process C, while is almost double (0.018 %) for the epoxy from Process A. Moreover, the shrinkage phenomenon occurs at a much higher temperature for Process C epoxy than for Process A (281 °C vs. 235 °C). These values are indicated in Fig. 3 a and b with arrows. That is, the dimensional change is less abrupt

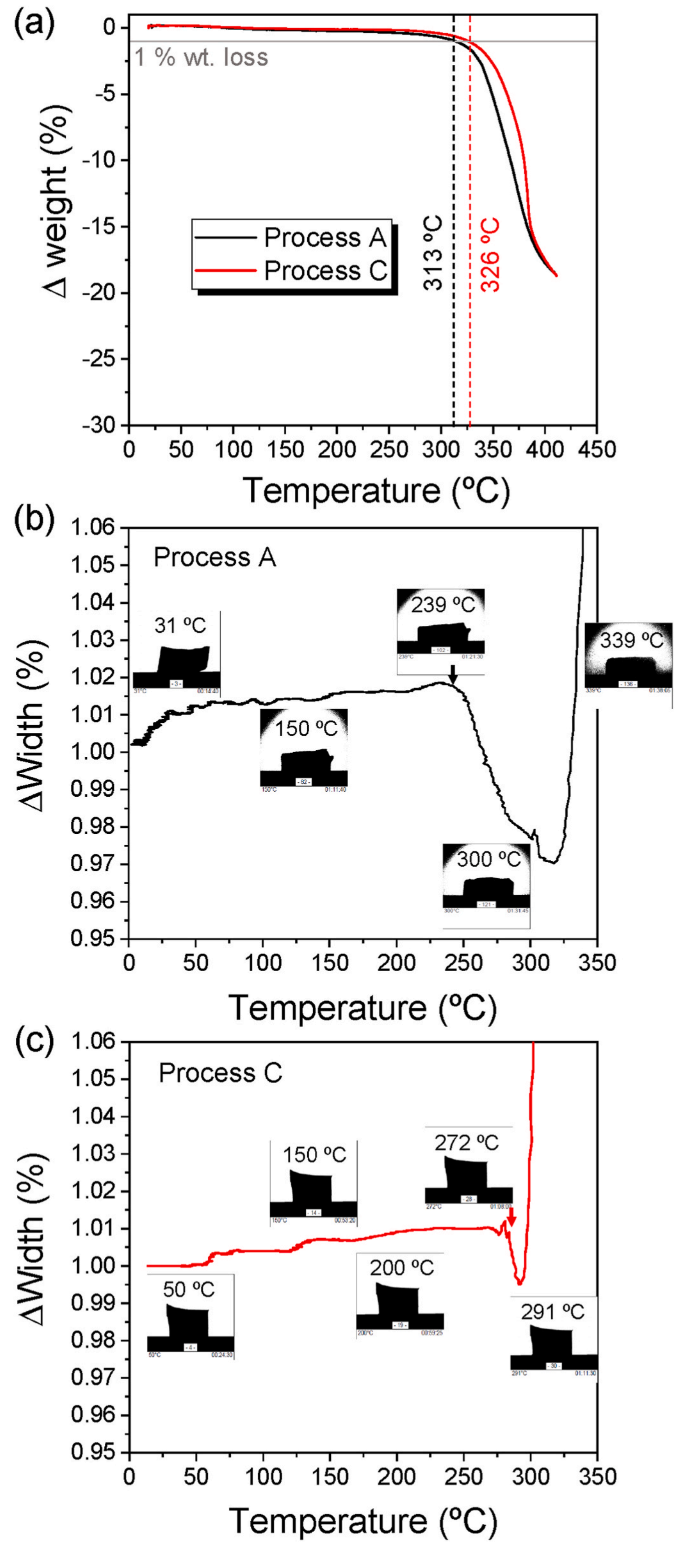

Fig. 3. **(a)** Thermogravimetric measurements of the Processes A and C epoxies, indicating onset temperature for 1 % wt. Loss. Dimensional change for the epoxies from **(b)** Process A and **(c)** Process C during the TGA experiment. For the epoxy from Process C, the onset of weight loss occurs at a higher temperature than the epoxy from Process A, and a lower rate of expansion at a higher temperature range is reached. Small arrows indicate the beginning of the shrinkage process for each diode.

and occurs during a larger temperature range for the epoxy from Process C, so a decrease in stress or strain level is expected. This shrinkage difference between diodes could be associated with unremoved pores during the epoxy potting step or void generated during curing, mainly coming from filler interfaces, indicating a greater relevance of this porosity evolution in Process A.

These modifications in the manufacturing of the diodes have a direct influence on their thermal behavior, which is investigated by infrared thermography experiments. Two experiments were carried out. In the first one, a continuous DC of 40 A was applied for 15 min (or up to failure, if applicable), registering the temperature in the epoxy region. This temperature is proportional to that reached in the Si chip and its evolution is representative of the different heating/heat release processes occurring in the diode. Fig. 4 shows an example of the

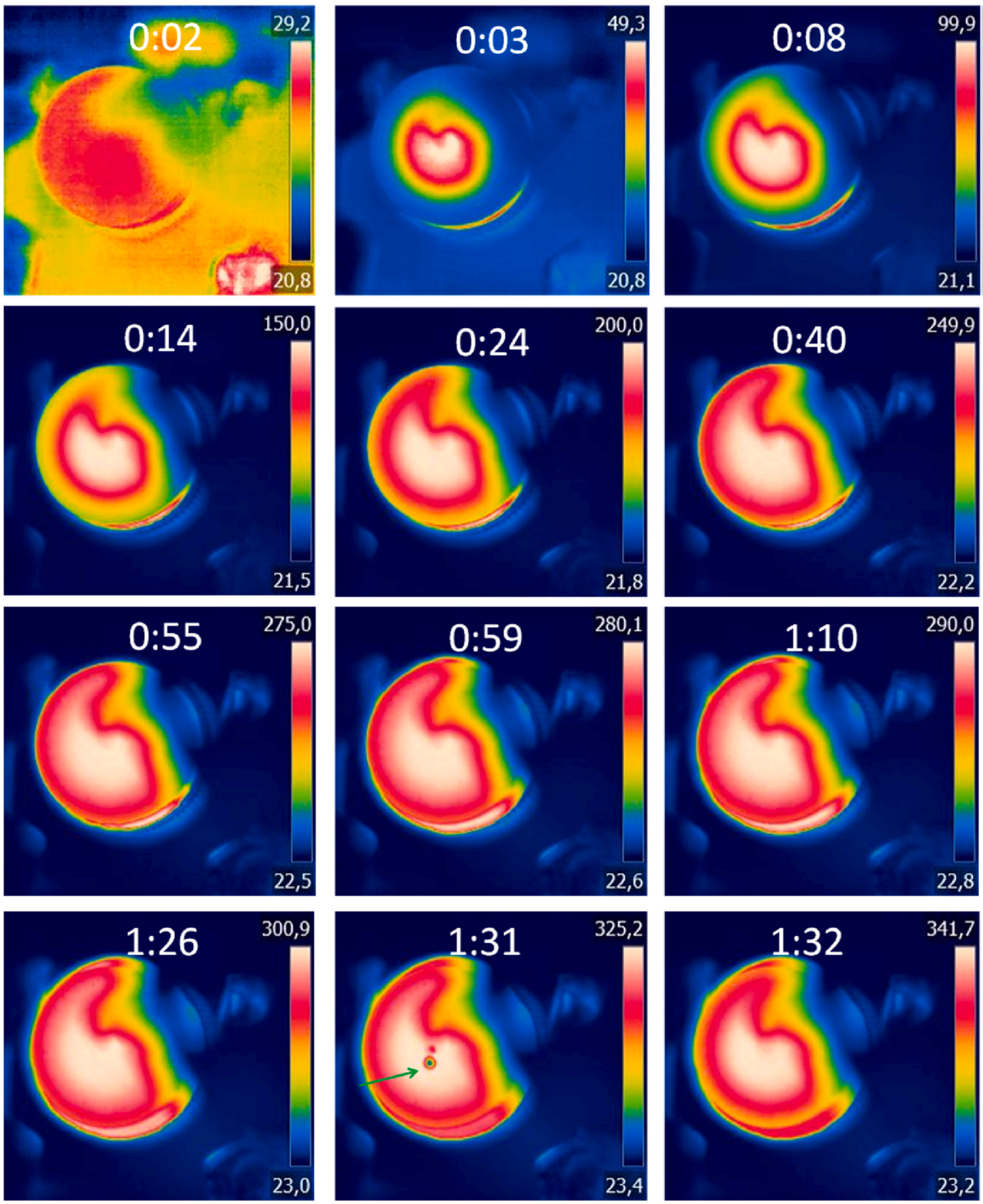

Fig. 4. Representative infrared thermography images of a positive diode from Process C at different times (expressed in minutes:seconds) while a current of 40 A is applied. Note the color scale changes as the heating time increases. In the thermography image taken at 1:31 min, the failure is caused by the melting of the solder indicated with an arrow. The color scale in each thermography image corresponds to the temperature signal indicating the values reached, in °C. Note that the right side of the thermograph images shows anomalies. This is due to the metal clamp used for the electrical connection generating a shadow effect that hinders the observation of the thermal image in this region.

thermography measurement of a diode from Process C, reflecting what was observed in the rest of the diodes. When the current is instantaneously increased from 0 to 40 A, a temperature rise is observed (Fig. 4, note the changes in the scales) up to a stabilization value that will depend on the electro-thermal response of the diode. From this point on, depending on the diode, two events can occur: (i) the temperature remains stable during the whole experiment time (15 min) and the diode does not undergo any change, and (ii) the diode may endure the negative consequences of the high temperature to which it is subjected. This event is observed in Fig. 4. Concretely, in the picture taken at 1:31 min, where solder melting is clearly distinguished through the epoxy, leading to the final failure of the diode.

The temperature at the epoxy was monitored for all the diodes and its evolution with time is shown in Fig. 5. After a current of 40 A was directly applied to the diodes in forward bias, a rapid increase of the silicon wafer temperatures due to the Joule effect occurs, which heats the epoxy component up to a certain stabilization temperature. Once the thermal stabilization is reached, some diodes can maintain that temperature up to the end of the experiment and other diodes may fail in times shorter than 15 min, as mentioned in the previous paragraph. The failures can be observed by a fast fall of temperature associated with the diode breakdown (i.e., diode 5- from Process A) or by a drop of temperature attributed to a failure in diode without mechanical break (i.e., diode 4+ from Process A). When the latter occurs, the diode does not work properly as a rectifier, but it is still capable of transporting the current across, producing heat by the Joule effect. The heating rate (considered as the time needed to reach a stabilization temperature of 250 °C measured at the external epoxy) and the time during which the device works correctly before failure are different for each diode. All these parameters are shown in Table 1.

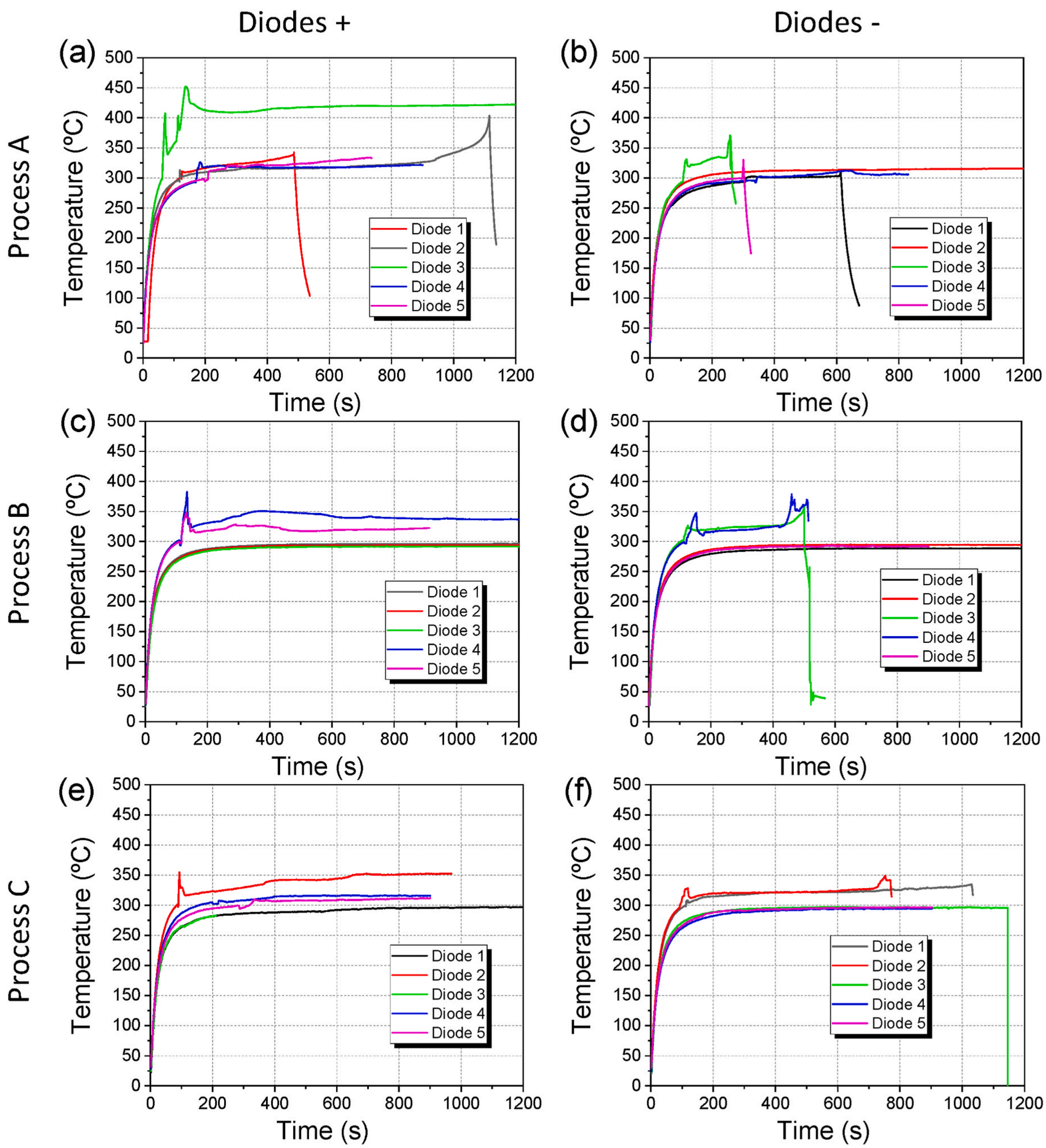

Fig. 5. Temperature-time dependence obtained from the thermography images of positive and negative diodes manufactured by processes A **(a–b)**, B **(c–d)**, and C **(e–f)**, while a current of 40 A was applied. From each process, a study of 5 diodes was performed. A drop in temperature occurs as each diode fails.

There are significant variations in the diode performance for the different processes. Process A diodes take the shortest times to reach 250 °C, with a significant difference of 10 s between positive and negative diodes, being the shortest times for the former than for the latter. Table 2 also shows that for positive diodes, an average time of 45 s is needed to reach the reference temperature (250 °C) for Process A, while this time increases more than 10 s to 56 and 57 s for Process B and C, respectively. Negative diodes need longer times to reach 250 °C but with the same trend: 55 s for Process A, 61 s for Process B, and 57 s for Process C. This means that the heating process at high currents is faster for Process A diodes, both positive and negative. This is reflected in the number of diodes which failed during the test. Only one of the 10 diodes tested for Process A could pass the test (did not break). As the failure occurs at shorter times for positive diodes in comparison to the negative ones, the number of diodes in this polarity that failed during the test also decreases. Half of the diodes continued working after 15 min and some of those that failed had quite high breaking times.

These results can be directly related to the solder characteristics. The measurements of the diode solder thickness shown in Fig. 2 and Table 1 point to a double drawback during the manufacturing process. On the one hand, the lack of control in the solder dimensions, leading to thickness lower than 20 μm, and, on the other hand, the lack of thickness homogeneity for diodes from process A, with wedges-shaped solders with differences in the thickness of more than 20 μm between the narrowest and widest regions. To study the influence of solder thickness in the heating of diodes as current is applied, we have modeled the thermal behavior of the diodes with different weld widths while subjected to an electrical forward current of 40 A (experimental conditions) for 50 s using COMSOL Multiphysics® software, as commented in the experimental section. To do that, we have set the conditions to simulate a temperature close to 250 °C (247 °C for the model) in the silicon wafer for a solder thickness of 80 μm. Then, we have kept the conditions of the simulation and just changed the solder thicknesses to 60, 40, and 20 μm aiming to assess the influence of this parameter. Fig. 6 shows the temperature distribution within each modeled diode changing the solder thickness as well as the maximum modeled temperature on the silicon chip and the modeled time needed to reach 250 °C when applying a 40 A current.

The increase of the diode temperature as the solder thickness decreases is clearly observed in Fig. 6a, having a linear relation in the concrete case of temperature of the silicon semiconductor (Fig. 6b). This result is mainly explained by the decrease in the thermal resistance of the solder with increasing thickness. In addition, a decrease in the times needed to reach 250 °C is obtained from simulations (measured in the epoxy but proportional to the heating in the silicon wafer) for thinner solders (Fig. 6c). As Table 2 shows, there seems to be a relation between shorter times to reach 250 °C in the epoxy and an increase in the failure rate. Therefore, heating simulations of rectifier diodes can help to explain the decrease in failure rates when changing from Process A to Process B (and C).

Table 2
Characteristic times for a continuous 40 A current test. The time needed to reach 250 °C and the time before failure for positive and negative diodes are shown for the three processes studied. Note that some diodes do not have breaking time since they worked properly during the whole experiment time.

		Time to 250 °C [s]	Breaking time [s]	Time to 250 °C [s]	Breaking time [s]
		Positive		Negative	
Process A	**1**	45	124	63	304
	2	31	117	47	–
	3	35	62	45	104
	4	58	161	61	337
	5	56	198	58	295
	Average	*45(6)*		*55(4)*	
Process B	**1**	60	–	77	–
	2	66	–	66	–
	3	69	–	46	112
	4	43	108	46	114
	5	44	109	72	–
	Average	*56(6)*		*61(6)*	
Process C	**1**	70	–	45	112
	2	40	87	42	92
	3	68	–	63	–
	4	51	199	76	–
	5	56	286	58	–
	Average	*57(6)*		*57(6)*	

It is clear that the reduced thermal resistance associated with a greater thickness in the solder favors the low temperature reached in the device after a long time of exposure to a high current. In addition, a complementary deduction can be inferred from these simulations. That is, the control in the manufacturing process aiming to have less wedged solders leads to a more homogenous heat distribution in the diode. Results displayed in Fig. 6 help to explain the diode behavior for wedged solders as those occurring in Process A diodes, although they have not been specifically modeled. The variation of thickness across the solder surface produces a non-homogenous temperature distribution in the silicon chip. The Joule effect associated with the current passing through the diode is responsible for heating the device. However, some regions (those near the thicker solder parts) reach lower temperatures than others (those near the thinner solder parts). As the forward voltage threshold (known as the voltage value at which the current starts flowing through the diode) decreases with temperature [27,28], current injection through the silicon chip will be favored at its hottest points. Subsequently, increasing the non-uniform heating of the solder and the Si chip will lead to a thermal runaway behavior that eventually produces the ending of the service lifetime of the diodes.

3.2. *Heating-cooling cycles*

In real application, diodes suffer continuous heating-cooling cycles that could lead to fatigue processes that ultimately may cause their failure, as stated before. Thus, an accelerated thermal cycling test characterized by an infrared thermography experiment has been carried out to understand these events and to follow the thermal evolution at critical points of the diodes. For the cycles, a temperature close to 250 °C was set in the sockets of each diode by applying the corresponding current (specific for each diode) for 2 min. Then, they were freely cooled for 2:30 min. Temperature was monitored at the external epoxy component close to the socket and the wire, for both positive and negative diodes. Figs. S2–S4 in supporting information show representative curves of the temperature measured at the selected points for the diodes manufactured by Processes A, B, and C, respectively. For each diode, the average of the socket-wire thermal gradient was averaged of all cycles was calculated. Fig. 7 shows representative thermographic images acquired at the maximum and minimum temperatures of a certain electric cycle of a diode from Process C (as representative) together with the gradient averaged for all the tested diodes.

The trends shown in this group of experiments indicate a remarkably high variance of thermal gradient values for Process A, showing positive and negative values. This means that for some diodes the hottest points are located in the socket and for others, they are located in the wire, in contrast to the trends observed in Process B and C, where they are mostly located in the socket. It is also noteworthy the quantitative differences between the gradient values of each type of diode. In Process A, the temperature gradients of some diodes reach absolute values close to 12 °C and others are about 0 °C. For Process B the gradient reaches values from 1 to 9 °C. Process C shows even more homogeneity in the thermal response between diodes, presenting values between 3 and 7 °C.

More homogeneous results are not directly related to a better performance of the diodes over thermal cycles in terms of durability. The efficiency of the devices is not only determined by thermal gradients but also by other factors related to thermoelastic phenomena due to the

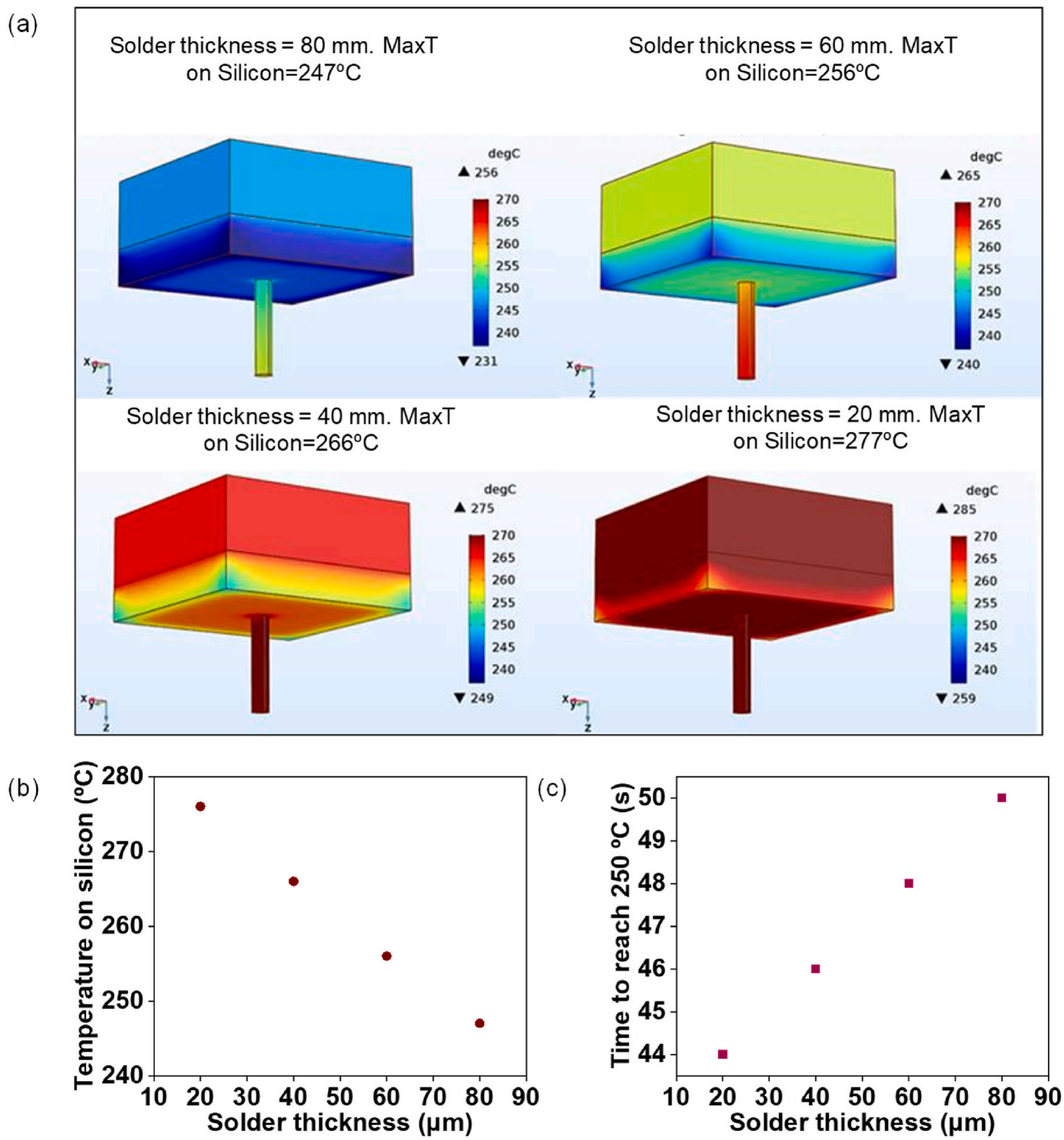

Fig. 6. (a) Modeled temperature distribution of forward bias diodes under the influence of a 40 A current applied for 50 s for different solder thicknesses:80, 60, 40, and 20 μm. **(b)** Calculated maximum temperature on the silicon chip and **(c)** time needed to reach 250 °C in the silicon wafer when applying 40 A as a function of solder thickness. Note that the color scale is individualized for each model, showing an increase in the temperature at decreasing solder thickness.

differences in expansion/contraction of each diode component (Si, solder, epoxy, and copper) that occur during the thermal heating/cooling cycles that lead to the appearance of interfacial stress. However, they are indeed a good indicator of improved diode construction through the modifications introduced in each process, which was proved through two facts. The first one is related to the manufacturing of the solder. As shown in previous sections, the reduction of the solder thickness and its inhomogeneity alter the heating process of the diode. Differences in thickness between the top and bottom solder as a result of a failure in diode construction give rise to variations in the heating rates of the socket and the wire. This explains that, in some cases, the hottest point is the socket and, in others, the wire, as observed in Fig. 7b, corresponding to Process A. By changing the manufacturing Process from A to B, less wedged and thicker solders are obtained, which results in better homogeneity in the temperature distributions, with sockets being the hottest part of the diodes in most cases. The second fact that was observed is that the epoxy component also plays a certain role in the thermal homogenization of the diode, so the proper choice of this component can help minimize the effects of solder characteristics in the heating of sockets and wire regions. Thus, the diodes obtained by Process C (optimized epoxy) present the lowest and most homogenous thermal gradients.

4. Conclusions

Optimization of some parameters of the different components of press-fit rectifier diodes during their fabrication process is essential to have devices with higher reliability and longer lifetimes. The use of epoxy resin with enhanced composition and a lower CTE is a key parameter to reduce stress at the interfaces of the device. Important heating variations have been proven to occur when modifying the solder manufacturing and/or when choosing a proper epoxy component. In

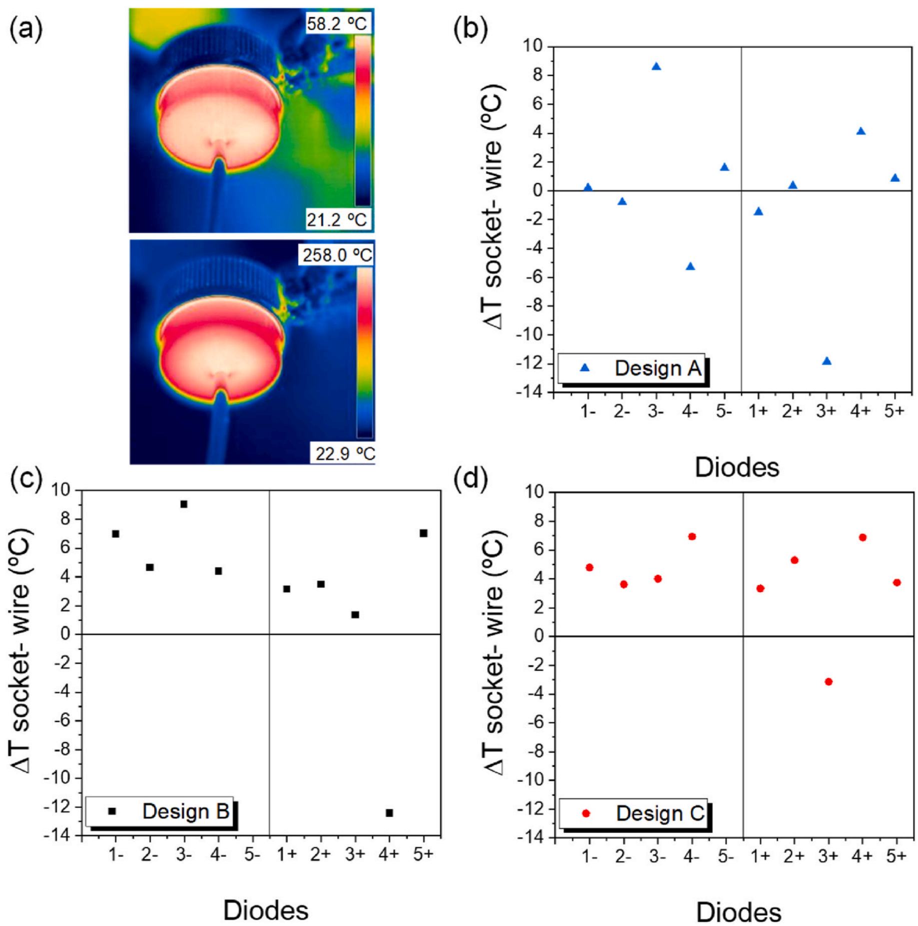

Fig. 7. **(a)** Infrared thermography images of a positive diode from Process C (as representative), at the maximum (bottom picture) and minimum (top picture) temperature reached during a thermal cycle. The color scale in each picture corresponds to the signal temperature indicating the values reached, in °C. Note the scale change between the images. Average thermal gradient occurring between the head-socket and the wire during the thermal cycles of diodes manufactured by **(b)** Process A, **(c)** Process B, and **(d)** Process C. The gradient of each diode was determined by subtracting the maximum wire temperature from the maximum head-socket temperature at each cycle and then averaging the values obtained from all cycles.

particular, thicker solders allow the diode to reach lower temperatures under operating conditions. In addition, a high homogeneity of the solder thickness improves the heat distribution and avoids thermal runaway effects that lead to total failure of the diode. Manufacturing control to obtain diodes with well-constructed solders and regulated dimensions prevents thermal gradients during cycling, which leads to an improved performance of the devices. All these factors: high-performance epoxy and thick and non-wedged solders result in an improved efficiency of the press-fit rectifier diodes, which provides a higher reliability and extends their service lifetime.

Competing financial interests

The authors declare no competing financial interest.

Data availability statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

Author contribution

All authors have approved the final version of the manuscript.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.jmrt.2023.12.155.

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